A8 circuit input terminal and said first circuit output terminal and a second capacitor is connected between said second circuit input terminal and said second circuit output terminal.

REMARKS

Claims 1-3, 5 and 7-9 are pending in the application. By this Amendment, Claims 1-3, 5 and 7-9 are amended, and Claims 4 and 6 are canceled without prejudice or disclaimer of the subject matter contained therein. Favorable reconsideration is respectfully requested in light of the following Remarks.

I. Formal Matters

1. The Office action objects to Figures 13, 14 and 15 asserting that Figures 13, 14 and 15 should be designated by a legend, such as "Prior Art." By this Amendment, a Request For Approval Of Drawing Corrections amending Figures 13, 14 and 15 to include the legend "Related Art" is attached hereto. Withdrawal of the objection is respectfully requested.

2. The Office action objects to the Figures 3 and 4 asserting that the plot of the conventional art when n=4 is illustrated by a legend with small circles, rather than the squares as described in the corresponding specification. By this Amendment, the corresponding specification has been amended to describe the plot of conventional art when n=4 with a legend of small circles to provide consistency between the description in the specification and the legend in Figures 3 and 4. Withdrawal of the objection is respectfully requested.

3. The Office action objects to Figure 6 asserting that the reference numerals for 21B and 22B are reverse. By this Amendment, a Request For Approval Of Drawing Corrections amending Figure 6 to reverse the reference numerals for 21B

and 22b is attached hereto. Withdrawal of the objection is respectfully requested.

4. The Office action objects to the specification asserting that the diodes Q2 and Q3, as shown in Figure 13, are connected parallel, rather than in series as described in the specification on Pages 7 and 8. By this Amendment, the specification has been amended to indicate that the diodes Q2 and Q3 are connected in parallel. Withdrawal of the objection is respectfully requested.

5. The Office Action objects to the specification asserting that the elements Q36-Q39, as described in the specification, are diode-connected transistors. By this Amendment, Page 26 of the specification is amended to indicate that the elements Q36-Q39 are transistors, rather than diode-connected transistors.

Although not mentioned in the Office action, the last paragraph of Page 30 spanning to Page 31 of the specification is also similarly amended to indicate that the elements Q56-Q59 are transistors, rather than diode-connected transistors. Withdrawal of the objection is respectfully requested.

6. The Office action asserts that the description on Page 40 of the specification is not understood. By this Amendment, the verbiage on Page 40 is deleted and should not have included in the originally-filed specification. Withdrawal of the objection is respectfully requested.

7. The Office action objects to Claims 1, 5 and 7 because of minor informalities. By this Amendment, Claims 1, 5 and 7 are amended to correct the minor informalities. Withdrawal of the objection is respectfully requested.

II. The Claims Satisfy the Requirements of 35 USC §112, First Paragraph

The Office action rejects Claim 2 under 35 USC §112, first paragraph asserting that it is not understood how a plurality of first and second differential circuits can be connected in series with each other between first and second power supplies, as recited in Claim 2. The rejection is respectfully traversed.

It appears that Claim 2 is supported by the specification. Referring to Figure 1, for example, the first differential circuits 15A and 16A are connected in series with each other, and the second differential circuits 16A and 16B are connected in series with each other. In addition, the first and second differential circuits are connected in series between a first power supply 13 and a second power supply 14. Thus, Claim 2 is supported by the specification and the rejection of Claim 2 is misplaced. It should be noted that Claim 2 may be supported by Figures 6 and 7 that illustrate modifications of Figure 1. Withdrawal of the rejection is respectfully requested.

III. The Claims Satisfy the Requirements of 35 USC §112, Second Paragraph

1. The Office action rejects Claim 3 under 35 USC §112, second paragraph asserting that it is not clear how the singular second differential circuit of Claim 3 can be connected in parallel to each of the plurality of first differential circuits. The rejection is respectfully traversed.

By this Amendment, Claim 3 is amended to specify that the second differential circuit is connected in parallel with at least one of the first differential circuits, rather than each

of the first differential circuits, as shown in Figures 1, 6 and 7. Withdrawal of the rejection is respectfully requested.

2. The Office action rejects Claim 4 under 35 USC §112, second paragraph asserting that it is not clear what "in series with each other" of Claim 4 refers to. The rejection is respectfully traversed.

By this Amendment, Claim 4 is essentially incorporated into Claim 1 and amended to specify that the second series connection circuit is formed by connecting a number of the second differential circuits in series with each other, as requested by the Office action. Withdrawal of the rejection is respectfully requested.

3. The Office action rejects Claims 6, 8 and 9 under 35 USC §112, second paragraph asserting that they are misleading and/or indefinite. By this Amendment, Claims 6, 8 and 9 are canceled, thereby rendering the rejection moot. Withdrawal of the rejection is respectfully requested.

IV. The Claims Define Patentable Subject Matter

The Office Action rejects Claims 1-9 under 35 USC 103(a) over Mihailovits et al. (U.S. Patent No. 5,847,605, hereinafter "Mihailovits"). The rejection is respectfully traversed.

Independent Claim 1 specifies, *inter alia*, a filter circuit including the feature of a first series connection circuit formed by connecting a plurality of first differential circuits in series with each other, is connected in parallel with a second series connection circuit formed by connecting a number of second differential circuits in series with each other, the number of the second differential circuits being identical with that of said first differential circuits of the

first series connection circuit, between a circuit input terminal and a circuit output terminal.

Mihailovits appears to disclose a third order filter circuit comprising three stages 260, 270 and 280. The first stage 260 comprises two differential transistor pairs 201, 202 and 203, 204 and a capacitor 240 connected across the output of the first stage. *See Fig. 2; col. 2, lines 30-38.* The second and third stages 270 and 280 have substantially the same layout as the first stage 260. *See col. 2, lines 38-40.* Each stage operates in substantially the same manner with the filter output being taken from the collector of transistors 210 and 211 of the final stage 280. *See col. 2, lines 43-46.*

To control the cutoff frequency electronically, a doublet, tunable low-pass filter circuit is provided comprising two offset differential pairs. The doublet filter circuit comprises a first pair of transistors 501, 502 having different emitter area, but the same emitter area as corresponding transistors 504, 503 in the opposite pair. The ratio of the emitter areas determines the offset voltage. *See Fig. 5; col. 3, lines 15-19; lines 42-55.*

Applicant agrees with the Office Action that Mihailovits does not disclose several aspects of the claimed invention. However, to overcome the shortcomings of Mihailovits, the Office Action asserts that it would have been obvious to modify the low-pass filter circuit of Mihailovits to meet the claimed invention. Applicant respectfully disagrees with this assertion.

The low-pass filter circuit of Mihailovits is directed to providing a cutoff frequency for the folded active filter of Mihailovits' Figure 2. To accomplish this, Mihailovits teaches a doublet circuit having a specific configuration of first and second transistor pairs with an emitter area ratio

that determines the offset voltage of between 4 and 5 and allows a linear response to input signals having a voltage swing of around 40 mv. *See col. 3, lines 45-49.*

By contrast, the claimed invention is directed to a filter circuit of low-voltage operation that can extend the input dynamic range while reducing current consumption comprising first and second differential circuits connected in parallel to each other through a capacitor. Thus, one skilled in the art would not look to the teachings of Mihailovits and modify the filter circuit of Mihailovits to meet the claimed invention, contrary to the Office action.

As admitted in the Office action, there is no mention whatsoever in Mihailovits of at least the feature of four parallel diode-connected transistors in a first differential circuit, and four parallel transistors in a second differential circuit connected by a capacitor. It should be noted that when a patent describes a new mechanical device that can be viewed as a new combination or arrangement of mechanical components, the legal conclusion of obviousness requires that there be some suggestion, motivation, or teaching in the prior art whereby the person of ordinary skill would have selected the components that the inventor selected and used them to make the new device. *See Heidelberger Druckmaschinen AG v. Hantscho Commercial Prods., Inc.*, 21 F.3d 1068, 1072, 30 USPQ 2d 1377, 1379 (Fed. Cir. 1993) ("When the patented invention is made by combining known components to achieve a new system, the prior art must provide a suggestion or motivation to make such a combination."); *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934, 15 USPQ 2d 1321, 1323 (Fed. Cir. 1990) (it is insufficient that prior art shows similar components, unless it also contains some teaching,

suggestion, or incentive for arriving at the claimed structure).[1]

In addition, determination of obviousness can not be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention. There must be a teaching or suggestion within the prior art, or within the general knowledge of a person of ordinary skill in the field of the invention, to look to particular sources of information, to select particular elements, and to combine them in the way they were combined by the inventor.[2]

Because Mihailovits does not disclose, teach or suggest all the claim limitations, as recited in Claim 1, and because there is no motivation in Mihailovits or to one of ordinary skill in the art at the time the invention was made to modify the filter circuit of Mihailovits, the Office Action fails to establish a *prima facie* case of obviousness. *See MPEP §2143.*

In view of the foregoing, it is respectfully submitted that Claim 1 is allowable over the applied art. Claims 2, 3, 5 and 7-9, which depend from Claim 1, are likewise allowable over the applied art. Withdrawal of the rejection is respectfully requested.

V. Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is earnestly solicited.

Should Examiner Englund believe anything further would be

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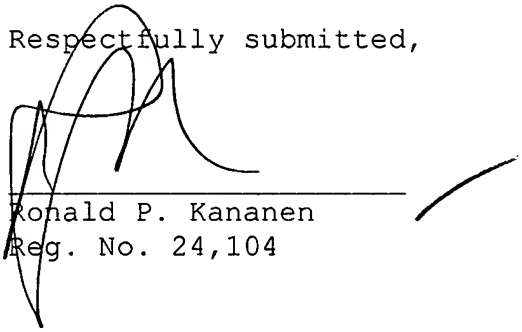
[1] *C.R. Bard, Inc. v. M3 Sys., Inc.*, 48 USPQ 2d 1225, 1231-32 (Fed. Cir. 1998).

[2] *ATD Corporation v. Lydall, Inc.*, 48 USPQ 2d 1321, 1329 (Fed. Cir. 1998).

desirable in order to place the application in better condition for allowance, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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MARKED UP VERSION OF ALL AMENDED SPECIFICATION PARAGRAPHS

First Full Paragraph On Page 2:

The base electrode and the collector electrode of the transistor Q2 are connected with a base electrode and a collector electrode of a transistor Q3. Thus, the transistor Q3 is also of the diode-connected configuration, and is connected in ~~series~~ parallel with the diode-connected transistor Q2 with a polarity opposite from the transistor Q2. A current source 112 is connected between the power supply line 103 and a common connection point of the bases and the collectors of the transistors Q2 and Q3. An emitter electrode of the transistor Q3 is connected with an emitter electrode of a transistor Q4. A current source 113 is connected between the GND line 104 and a common emitter connection point of the transistors Q3 and Q4.

Last Paragraph On Page 16 spanning to Page 17:

FIG. 3 shows characteristics of the current IO with respect to the input vi. In the characteristic diagram of FIG. 3, a curve indicated by alternate long and short dashed lines plotted by a mark of ⊟ O represents a characteristic of the conventional circuit of FIG. 13 when n = 4; a curve indicated by a broken line plotted by a mark of O represents a characteristic of the conventional circuit of FIG. 14 when n = 3; and a curve indicated by a solid line plotted by a mark of × represents a characteristic of the circuit according to the first embodiment. As is clear from the characteristic diagram, linearity of the current IO of the circuit according to the first embodiment is better than that of the circuits according to the conventional examples.

Last Paragraph On Page 17 spanning to Page 18:

FIG. 4 shows input-output characteristics when an input frequency f is f = fc. FIG. 5 shows distortion factor (T. H. D.) characteristics when f = fc. Also in these characteristic diagrams, a curve indicated by alternate long and short dashed lines plotted by a mark of ⊟—O represents a characteristic of the conventional circuit of FIG. 13 when n = 4; a curve indicated by a broken line plotted by a mark of O represents a characteristic of the conventional circuit of FIG. 14 when n = 3; and a curve indicated by a solid line plotted by a mark of × represents a characteristic of the circuit according to the first embodiment. As is clear from the characteristic diagram of FIG. 4, linearity of the input-output characteristic of the circuit according to the first embodiment is better than that of the circuits according to the conventional examples. As is clear from the characteristic diagram of FIG. 5, the circuit according to the first embodiment has a distortion factor better than those of the circuits according to the conventional examples within a range of 0.9% or less.

Last Paragraph On Page 26:

On the other hand, a second differential circuit 36A is formed by four ~~diode-connected~~ transistors Q36 to Q39 connected in parallel with each other and a diode-connected transistor Q40 having an emitter electrode connected to each of emitter electrodes of the transistors Q36 to Q39. A current source 42A is connected between a common emitter connection point of the transistors Q36 to Q40 and the GND line 34.

Last Paragraph On Page 30 spanning to Page 31:

On the other hand, a second differential circuit 56A is formed by four ~~diode-connected~~ transistors Q56 to Q59 connected in parallel with each other and each having a base electrode connected to the circuit input terminal 51 and a diode-connected transistor Q60 having an emitter electrode connected to each of emitter electrodes of the transistors Q56 to Q59. A current source 62A is connected between a common emitter connection point of the transistors Q56 to Q60 and the GND line 54.

Page 40:

~~FIG. 1~~

~~15A, 15B: FIRST DIFFERENTIAL CIRCUIT~~

~~16A, 16B: SECOND DIFFERENTIAL CIRCUIT~~

~~FIGs. 3, 4, 5~~

~~3-1: CONVENTIONAL CIRCUIT~~

~~3-2: CIRCUIT OF PRESENT INVENTION~~

MARKED UP VERSION OF ALL AMENDED CLAIMS

1. A filter circuit comprising:

a first differential circuit formed by a combination of one transistor, and four diodes connected in parallel with each other and each having one electrode connected to a first electrode of said one transistor, a first current corresponding to an input signal flowing through said four diodes;

a second differential circuit formed by a combination of one diode, and four transistors connected in parallel with each other and each having a first electrode connected to one electrode of said one diode, a second current corresponding to the input signal flowing through said one diode;

a current source connected to a common connection point of said four diodes and said one diode; and

a first capacitor through which a current determined by a current of said current source, said first current, and said second current flows,

wherein a first series connection circuit formed by connecting a plurality of said first differential circuits in series with each other is connected in parallel with a second series connection circuit formed by connecting a number of said second differential circuits in series with each other, the number of said second differential circuits being identical with that of said first differential circuits of said first series connection circuit, between a circuit input terminal and a circuit output terminal.

2. A filter circuit as claimed in claim 1,

wherein ~~a~~ the plurality of said first differential circuits are connected in series with each other and ~~a~~ the

plurality of said second differential circuits are connected in series with each other between a first power supply and a second power supply.

3. A filter circuit as claimed in claim 1,

wherein a plurality of said first differential circuits are connected in series with each other between a circuit input terminal and a circuit output terminal; and

said second differential circuit is connected in parallel with ~~each~~ at least one of said first differential circuits.

5. A filter circuit as claimed in claim 1,

wherein a control electrode of said one transistor and control electrodes of said four transistors are connected to a first circuit input terminal, and the common connection ~~node~~ point of said four diodes and said one diode is connected to a first circuit output terminal; and

one terminal of said first capacitor is connected to said first circuit output terminal.

7. A filter circuit as claimed in claim 1,

wherein a control electrode of said one transistor and control electrodes of said four transistors are connected to a direct-current power supply, and the common connection ~~node~~ point of said four diodes and said one diode is connected to a first circuit output terminal; and

said first capacitor is connected between a first circuit input terminal and said first circuit output terminal.

8. A filter circuit as claimed in claim 7,

wherein said first differential circuit, said second

differential circuit, and said current source are further provided between said direct-current power supply and a second circuit output terminal; and

~~said~~ a second capacitor is connected ~~also~~ between a second circuit input terminal and said second circuit output terminal.

9. A filter circuit as claimed in claim 1,

wherein a control electrode of said one transistor and control electrodes of said four transistors are connected to a first circuit input terminal, the common connection point of said four diodes and said one diode is connected to a second circuit output terminal, and said first differential circuit, said second differential circuit, and said current source are provided also between a second circuit input terminal and a first circuit output terminal; and

said first capacitor is connected between said first circuit input terminal and said first circuit output terminal and a second capacitor is connected between said second circuit input terminal and said second circuit output terminal.